Materials Science Forum Vols. 600-603 (2009) pp 1079-1082
online at http://www.scientific.net

Fabrication and Testing of 6H-SiC JFETs for Prolonged 500 °C Operation in Air Ambient

David J. Spry[1,a], Philip G. Neudeck[2,b], Liang-Yu Chen[1,c], Glenn M. Beheim[2], Robert S. Okojie[2], Carl W. Chang[3], Roger D. Meredith[2], Terry L. Ferrier[2], and Laura J. Evans[2]

[1]OAI, NASA Glenn, 21000 Brookpark Road, M.S. 77-1, Cleveland, OH 44135 USA

[2]NASA Glenn Research Center, 21000 Brookpark Road, M.S. 77-1, Cleveland, OH 44135 USA

[3]ASRC Aerospace Corporation, 21000 Brookpark Road, M.S. 77-1, Cleveland, OH 44135 USA

[a]David.J.Spry@nasa.gov, [b]Philip.G.Neudeck@nasa.gov, [c]Liangyu.Chen@grc.nasa.gov

Keywords: 6H-SiC, JFET, Junction Field Effect, Transistor, Durability, Reliability, High Temperature, Amplifier, Differential Amplifier, and Packaging.

Abstract: This paper reports on the fabrication and testing of 6H-SiC junction field effect transistors (JFETs) and a simple differential amplifier integrated circuit that have demonstrated 2000 hours of electrical operation at 500 °C without degradation. The high-temperature ohmic contacts, dielectric passivation, and packaging technology that enabled such 500 °C durability are briefly described. Key JFET parameters of threshold voltage, on-state resistance, transconductance, and on-state current, as well as the gain of the differential amplifier integrated circuit, exhibited less than 7% change over the first 2000 hours of 500 °C operational testing.

Introduction

Extension of the operating temperature envelope of semiconductor transistor integrated circuits well above the effective 300 °C limit of silicon-on-insulator technology should enable significant improvements to aerospace, automotive, energy production, and other industrial systems [1]. Last year, NASA reported a 6H-SiC metal semiconductor field effect transistor (MESFET) and an inverting amplifier (constructed from discrete resistors, capacitors and a transistor) that both demonstrated prolonged electrical operation (over 1000 hours at 500°C [2, 3]). However, these MESFET's suffered from incomplete turn-off of channel current and gradually increasing leakage of the metal-semiconductor gate-to-channel junction that led to device degradation and failure. This paper reports 6H-SiC JFETs that do not suffer from the above problems, and their use to implement a differential amplifier integrated circuit chip that has electrically operated for over 2000 hours at 500 °C in air atmosphere without degradation. This establishes a technology foundation for realizing durable 500 °C harsh-environment integrated circuits.

Experimental

A quarter wafer of small-signal 6H-SiC JFET's and single-layer metal interconnect to form integrated circuits was fabricated starting from commercially [4] purchased epilayered substrates. Figure 1 shows the simplified cross-sectional schematic of the basic JFET device structure that was fabricated. Following

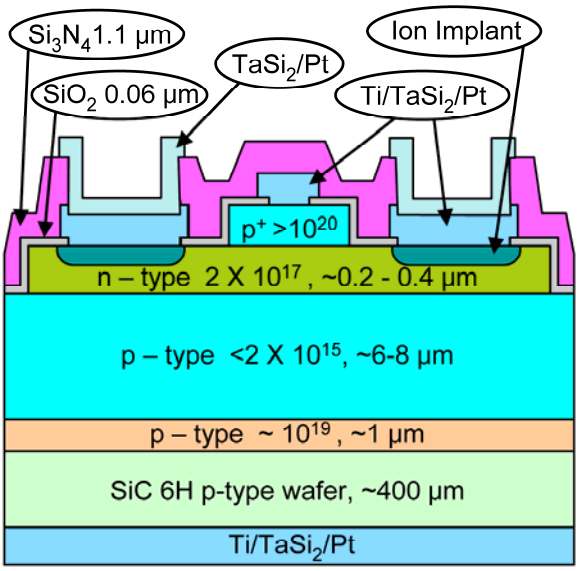

Fig. 1. Simplified schematic cross-section of 6H-SiC JFET. The n-type layer was used for resistors in integrated circuits.

patterned dry-etch definition of the JFET p^+ gate and n-channel, the n-type channel was nitrogen-implanted (same implant specifications as [3]) to form the heavily-doped source-drain contact regions. The n-type implant was activated uncapped for 30 minutes in 150 torr argon at 1200 °C. A 600 Å thick oxide was grown via thermal oxidation process of Lipkin et al [5], followed by a patterned oxide via etch. The highly durable n-ohmic metallization scheme of Ti/$TaSi_2$/Pt reported by Okojie et al [6] was deposited as contacts to both n-type source/drain implants as well as the heavily p-type-doped gate epilayer. Both the contact and the subsequent interconnect metal layer were patterned by a combination dry/wet etch process in order to minimize the possibility of dry-plasma ion damage to dielectric layers. In particular, dry-etching first removed most of the field metal from regions not protected by the photoresist pattern, followed by a brief wet etch that removed the remaining field metal. 1.1µm-thick Si_3N_4 was deposited using reactive sputtering. Vias were fabricated with dry-etching through the nitride to the underlying ohmic metallizations. The top interconnect/bondpad metal layer was then patterned by the combination dry/wet etch process. A brief 15 minute etch in 1 H_2SO_4 : 1 H_2O_2 was used to clean the sample in preparation for dicing and packaging.

Almost all JFET's and integrated circuits probe-tested on the quarter-wafer functioned at room temperature. Brief probe-station tests of a few diced chips were carried out at 500 °C using a heated sample stage. The probe-station tested devices also demonstrated excellent performance. However, probe-testing is not viable for carrying out long-term 500 °C operational electrical testing, as significant oxidation and vibration induced probe-tip degradation occurs over time at that temperature.

Several chips from the wafer were selected for an initial round of packaging and long term 500 °C electrical testing. The chips were packaged in custom packages resembling a standard Ceramic Dual In-line Package (CERDIP) but made only with aluminum oxide and Au-thick film metallization as previously reported [7]. The packaged chips were mounted on an alumina high temperature circuit board [7]. The circuit board was placed into a table top oven with attached unshielded Au wires leads running from the circuit board to electrical test instruments outside the oven. The devices and integrated circuit reported in this paper are only intended to demonstrate prolonged operational durability at 500 °C instead of optimal electrical performance. The amplifier circuit outputs were wired to AC-coupled oscilloscope probe inputs with 10 MΩ, 11 pF input impedance. Computer-controlled power supplies, source-measure units, digitizing curve tracers, and digitizing oscilloscopes were employed to continuously apply bias and measure electrical characteristics of the devices throughout the 500 °C test. The atmosphere inside the oven was ordinary room air, which normally contains 21% oxygen and an average monthly humidity as high as 86% during the summer.

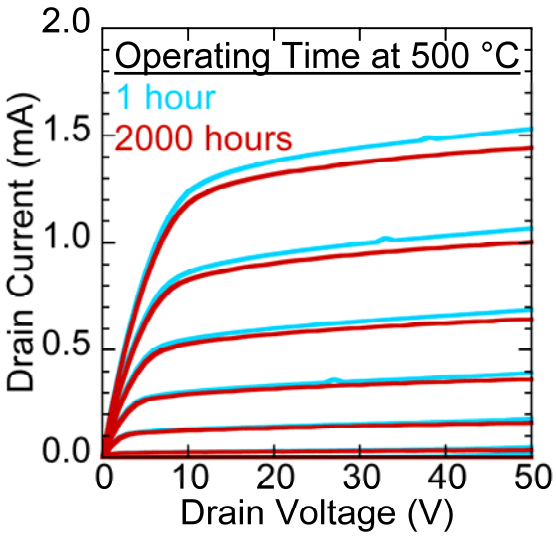

Fig. 2. Drain I-V characteristics of packaged 200µm/10µm 6H-SiC JFET at 1st and 2000th hour of electrical testing at 500°C. Gate steps are -2V starting from V_G = 0V with the source and substrate grounded.

Results

As the results presented in Figs. 2-6 summarize, excellent long-term 500 °C operational durability was demonstrated for both the discrete JFET transistor and integrated differential amplifier circuit. Figure 2 shows almost no difference between the 200µm/10µm

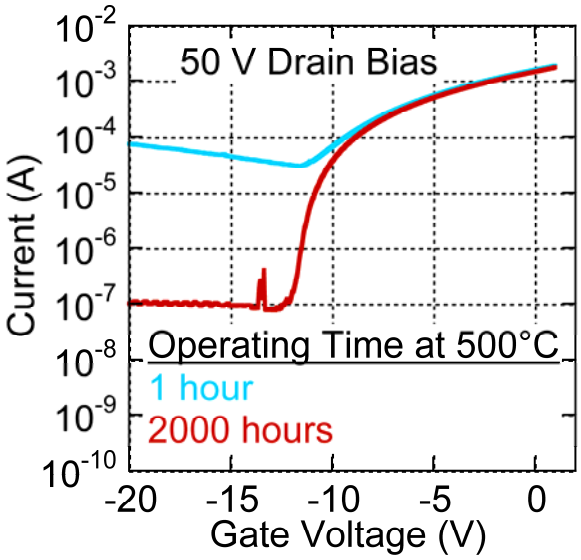

Fig. 3. Drain current (log scale) vs. gate voltage characteristics of the 200µm/10µm 6H-SiC JFET at 1st and 2000th hour of electrical testing at 500°C for V_D = 50V.

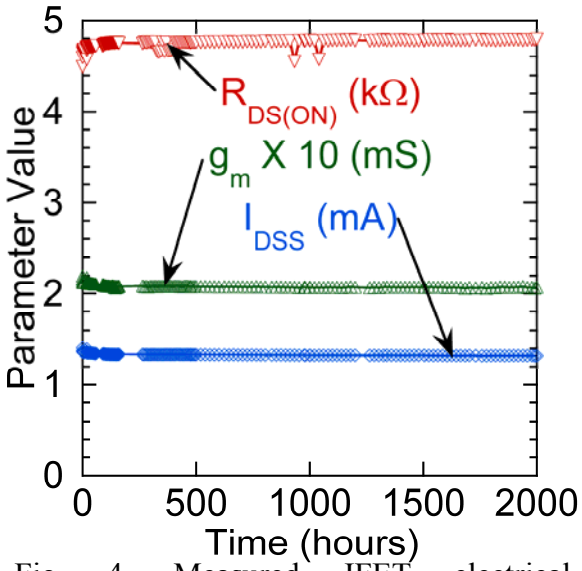

Fig. 4. Measured JFET electrical parameters vs. operating time at 500°C. $R_{DS(ON)}$, g_m at V_G = -1V, V_D = 20V, and I_{DSS} at V_G = 0V, V_D = 20V.

JFET drain current versus drain voltage characteristics recorded at the beginning (1st hour) and end (2000th hour) of 500 °C operation under DC stress of V_D = 50 V and V_G = -6 V. A 100µm/10µm JFET exhibited similar results. Figure 3 shows the corresponding drain current (log scale) versus gate voltage data (at V_D = 50 V) recorded for the same 200µm/10µm JFET. The turn-off current (in V_G < -12 V sub-threshold region) improves (i.e., is reduced) by over an order of magnitude by the end 2000 hours of the testing. This is believed to be due to improved insulation performance of the nitride dielectric coating the device as the 500 °C test in air ambient proceeds. A separate measurement of a nitride dielectric capacitor test structure (not shown) exhibited similar improvement. For both the transistor and the test capacitor, most of the improvement in leakage current occurred during the first 100 hours of 500 °C testing.

Figure 4 plots the values of transistor on-state resistance (R_{DS} measured at V_G = 0), transconductance (g_m measured at V_G = -1 V, V_D = 20V), and on-state current I_{DSS} (I_D measured at V_G = 0, V_D = 20 V) extracted from measured 500 °C test data. The variation of all these important transistor parameters over the course of the 2000 hour 500 °C operational test is less than 7%. The gate leakage current (I_G measured at V_G = -5 V, V_D = 50 V) was 8.6 µA at the start of the test, and improved (i.e., reduced) about two orders of magnitude to 0.07 µA by the end of the test. The change in threshold voltage V_T is not plotted in Fig. 4 because it is less than 0.05 V. Though very small, the majority of parameter variations also occurred during the first 100 hours of the test.

Figure 5 shows the circuit schematic of the simple resistive load circuit that was primarily intended to demonstrate interconnect/integration material and process durability. Figure 6 summarizes the 500 °C durability testing of the differential amplifier integrated circuit. Figure 6 illustrates that nearly identical gain versus frequency characteristics are measured at the start and end of the 2000 hour 500 °C operational test. The outstanding high temperature durability of the circuit is demonstrated by the fact that the amplifier performance at the beginning and end of the test are virtually identical.

Summary Discussion

As of this writing, operational testing of the above JFET and differential amplifier integrated circuit in the 500 °C oven beyond 2000 hours is ongoing. 500 °C durability testing of additional devices has also been initiated as additional testing equipment (ovens and instruments) and packaged parts have

become available. Presently 500 °C testing is being performed on three metal-insulator-semiconductor capacitors, a second discrete JFET, a pair of digital logic gate integrated circuits and an integrated inverting amplifier stage. Results of these tests, including the only observed circuit failure that we speculate was due to excessive power supply voltage applied in that test, will be reported in the future.

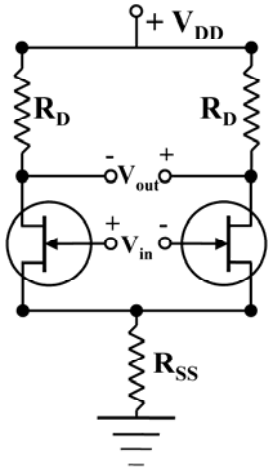

Fig. 5. Diagram of differential amplifier integrated circuit operated at 500°C. V_{DD} = 40V and $R_D = R_{SS}$ = 545Ω.

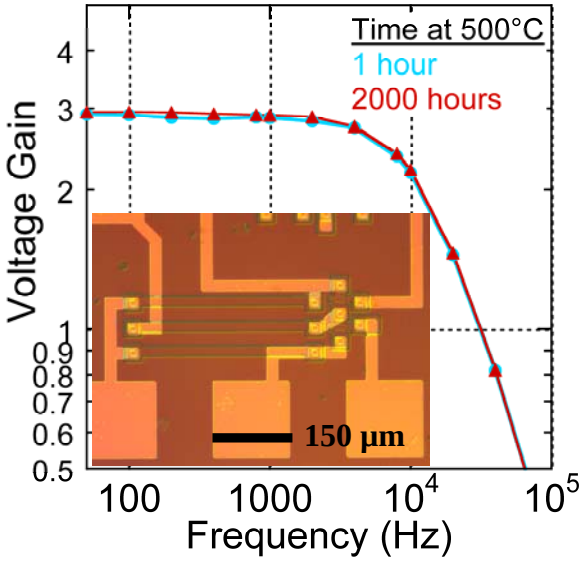

Fig. 6. Differential amplifier measured gain vs. frequency measured during the 1st and 2000th hour of 500°C operation. Inset shows optical photograph of diff-amp chip recorded during probe-testing.

Although only a small number of devices have been packaged and tested to date, the results establish clear experimental feasibility that simple SiC integrated circuitry capable of prolonged 500 °C can be implemented. This result was achieved through the non-trivial integration of several fundamental materials and/or processing advancements, including the development of high temperature n-type ohmic contacts [6] and high temperature packaging technology [7]. The choice of junction FET technology and its designed operation at relatively low electric fields and currents are also believed crucial to these achieved results.

The demonstrated 2000 hour 500 °C durability is sufficient for sensor signal conditioning circuits to survive most jet-engine ground test programs. However, far greater circuit complexity than the basic integrated circuits with a few-transistors demonstrated in this initial work is needed for most envisioned applications. Following the technology evolution of past silicon integrated circuitry, scale-up to more complex 500 °C SiC integrated circuitry will clearly involve shrinkage of device dimensions and operating biases as well as implementation of multilayer interconnects.

Acknowledgements

This work is presently funded by the NASA Aeronautics Research Mission Directorate in both the Aviation Safety and Fundamental Aeronautics Programs under the Integrated Vehicle Health Management, Subsonic Fixed Wing, and Supersonics Projects. Prior-year NASA funding for this work included the Glennan Microsystems Initiative, Ultra Efficient Engine Technology, Propulsion 21, and NASA electronics Parts and Packaging programs. Work was carried out by NASA Glenn Research Center with assistance of D. Lukco, A. Trunek, D. Androjna, K. Laster, J. Gonzalez, R. Lotenero, M. Mrdenovich, B. Osborn, G. Hunter, and L. Matus.

References

[1] P. G. Neudeck, R. S. Okojie, and L.Y. Chen Proc. of IEEE, 90, p. 1065 (2002).
[2] P. G. Neudeck et al.: Materials Sci. Forum 556-557, p. 831 (2007).
[3] D. J. Spry, et al.: Proc. 2004 IMAPS Int. Conf. High Temperature Electronics, p. WA1.
[4] Cree Inc.: http://www.cree.com
[5] L. A. Lipkin, et al.: Journal of Electronic Materials 25, p.909 (1996).
[6] R. S. Okojie, et al.: Mat. Res. Soc. Symp. Proc. 622, p. H7.5.1 (2000).
[7] L. Y. Chen, et al.: Proc. 2006 IMAPS Int. Conf. High Temperature Electronics, p. 240.